WHAT IS CLAIMED IS:

1. A random access memory device comprising:

a controller;

a data bus coupled to the controller such that data read and data write information is transferred to and from the controller over the data bus;

multiple memory modules coupled to the data bus and to the controller, each memory module having a driver that produces an echo clock signal on an echo clock pin, the echo clock pin of each memory module being tied to each of the other memory modules and to the controller, such that during a read operation of the random access memory device the data bus and echo clock have matched loading conditions.

2. The random access memory device of claim 1 wherein each memory module further includes a buffer.

3. The random access memory device of claim 2 wherein the echo clock pin of each memory module is tied to the buffer of each of the other memory modules.

4. The random access memory device of claim 3 wherein the buffer is an unused buffer resulting from the memory module using less than it full capacity.

5. The random access memory device of claim 3 wherein the buffer is a dummy buffer added to the memory module.

6. The random access memory device of claim 2 wherein the random access memory device includes a first and a second memory module coupled to the data bus, the first memory module having a first echo clock driver producing a first echo clock signal and having a first buffer, the second memory module having a second echo clock driver producing a second echo clock signal and having a

second buffer, wherein the first echo clock signal is coupled to the controller and to the second buffer and the second echo clock signal is coupled to the controller and to the first buffer such that during a read operation of the random access memory device the data bus and the first and second echo clocks have matched loading conditions.

7. The random access memory device of claim 2 wherein the random access memory device includes a first, second, third and fourth memory module coupled to the data bus, the first memory module having a first echo clock driver producing a first echo clock signal and having a first buffer, the second memory module having a second echo clock driver producing a second echo clock signal and having a second buffer, the third memory module having a third echo clock driver producing a third echo clock signal and having a third buffer, the fourth memory module having a fourth echo clock driver producing a fourth echo clock signal and having a fourth buffer, wherein the first echo clock signal is coupled to the controller and to the second, third and fourth buffers, the second echo clock signal is coupled to the controller and to the first, third and fourth buffers, the third echo clock signal is coupled to the controller and to the first, second and fourth buffers, and the fourth echo clock signal is coupled to the controller and to the first, second and third buffers such that during a read operation of the random access memory device the data bus and the first, second, third and fourth echo clocks have matched loading conditions.

8. A random access memory device comprising:

a controller;

a data bus coupled to the controller such that data read and data write information is transferred to and from the controller over the data bus;

a first memory module coupled to the data bus and to the controller, the first memory module having a driver that generates an echo clock signal and having a buffer;

a second memory module coupled to the data bus and to the controller, the second memory module having a driver that generates an echo clock signal and having a buffer, the echo clock signal of the second memory module being tied to the buffer of the first memory module and to the controller, the echo clock signal of the first memory module being tied to the buffer of the second memory module and to the controller.

9. The random access memory device of claim 8 wherein the buffers of the first and second memory modules are off and producing a load, such that during a read operation of the random access memory device the data bus and echo clock of the first memory module have matched loading conditions.

10. The random access memory device of claim 8 wherein the buffers of the first and second memory module are off and producing a load, such that during a read operation of the random access memory device the data bus and echo clock of the second memory module have matched loading conditions.

11. The random access memory device of claim 8 wherein the buffer is an unused buffer from the memory module using less than it full capacity.

12. The random access memory device of claim 8 wherein the buffer is a dummy buffer added to the memory module.

13. The random access memory device of claim 8 further including a third memory module coupled to the data bus and to the controller, the third memory module having a driver that generates an echo clock signal and having a buffer, the echo clock signal of the first memory module being tied to the buffers of the second and third memory modules and to the controller, the echo clock signal of the second memory module being tied to the buffers of the first and third memory modules and to the controller, and the echo clock signal of the third

memory module being tied to the buffers of the first and second memory modules and to the controller.

14. The random access memory device of claim 13 wherein the buffers of the first, second and third memory modules are off and producing a load, such that during a read operation of the random access memory device the data bus and each echo clock have matched loading conditions.

15. The random access memory device of claim 13 further including a fourth memory module coupled to the data bus and to the controller, the fourth memory module having a driver that generates an echo clock signal and having a buffer, the echo clock signal of the first memory module being tied to the buffers of the second, third, and fourth memory modules and to the controller, the echo clock signal of the second memory module being tied to the buffers of the first, third, and fourth memory modules and to the controller, the echo clock signal of the third memory module being tied to the buffers of the first, second, and fourth memory modules and to the controller, and the echo clock signal of the fourth memory module being tied to the buffers of the first, second, and third memory modules and to the controller.

16. The random access memory device of claim 15 wherein the buffers of the first, second third and fourth memory modules are off and producing a load, such that during a read operation of the random access memory device the data bus and each echo clock have matched loading conditions.

17. A random access memory device comprising:

a controller;

a data bus coupled to the controller such that data read and data write information is transferred to and from the controller over the data bus;

multiple memory modules coupled to the data bus and to the controller, each memory module producing an echo clock signal that is received by the

controller during a read operation of the random access memory device and each memory module including means for matching the loading conditions of the data bus and the memory modules.

18. The random access memory device of claim 18 wherein each memory module has a driver that produces an echo clock signal, the echo clock signal of each memory module being received by each of the other memory modules and by the controller, such that during a read operation of the random access memory device the data bus and echo clock have matched loading conditions.